F I G. 1

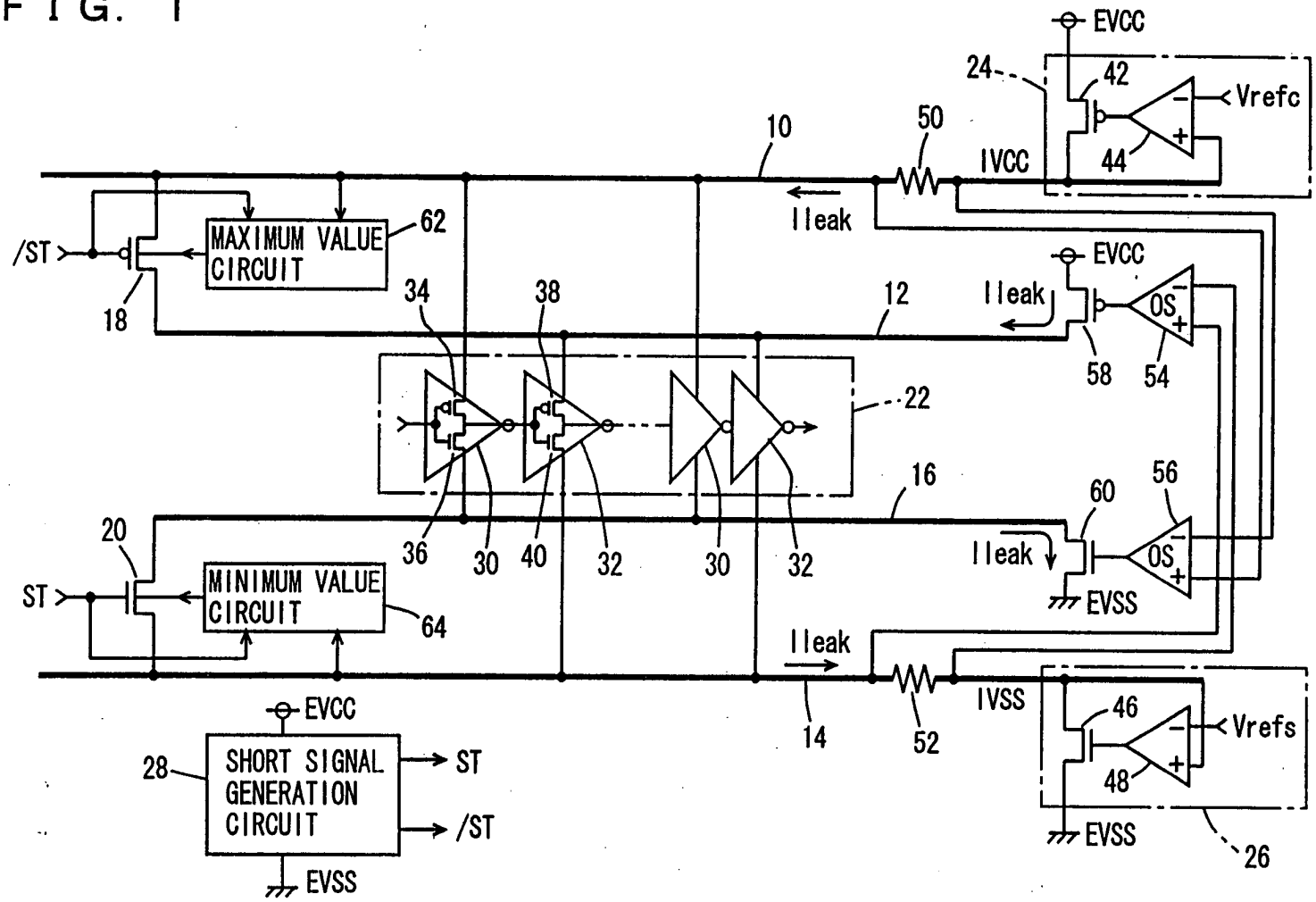

EVCC
24
42
Vrefc
44
10
50
IVCC
Ileak
/ST
MAXIMUM VALUE CIRCUIT
62
18
EVCC
Ileak
OS
12
58
54
34
38
22
16
60
56
20
36
30
40
32
30
32
Ileak
OS
ST
MINIMUM VALUE CIRCUIT
64
EVSS
Ileak
IVSS
14
52
46
Vrefs
48
EVCC
28
SHORT SIGNAL GENERATION CIRCUIT
ST
/ST
EVSS
EVSS
26

FIG. 2

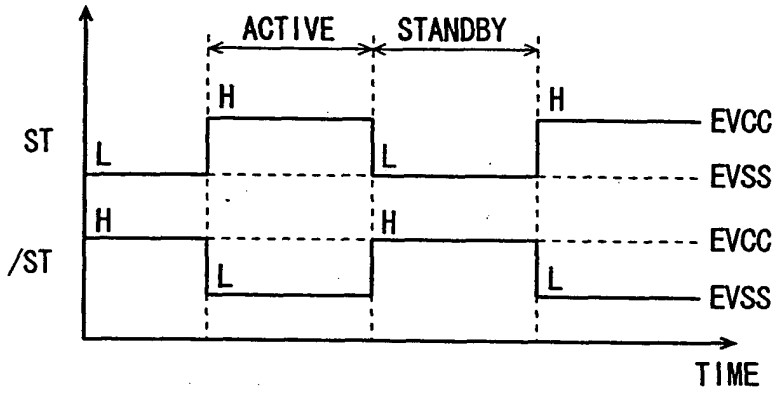


FIG. 3

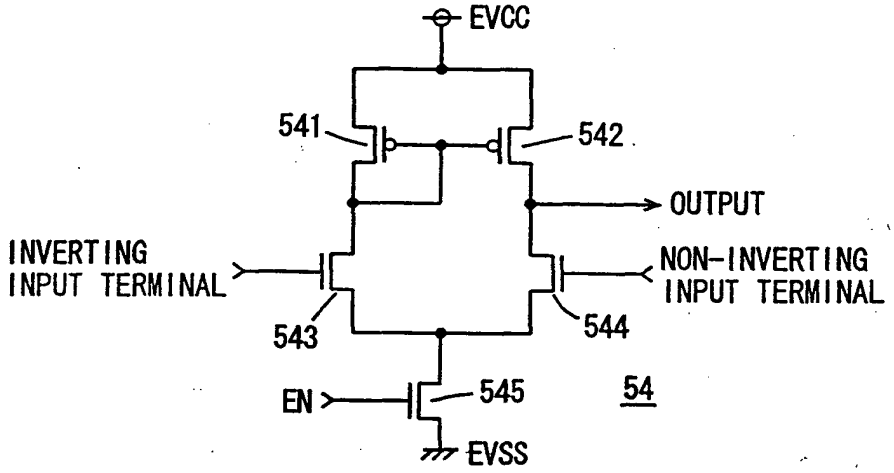


FIG. 4

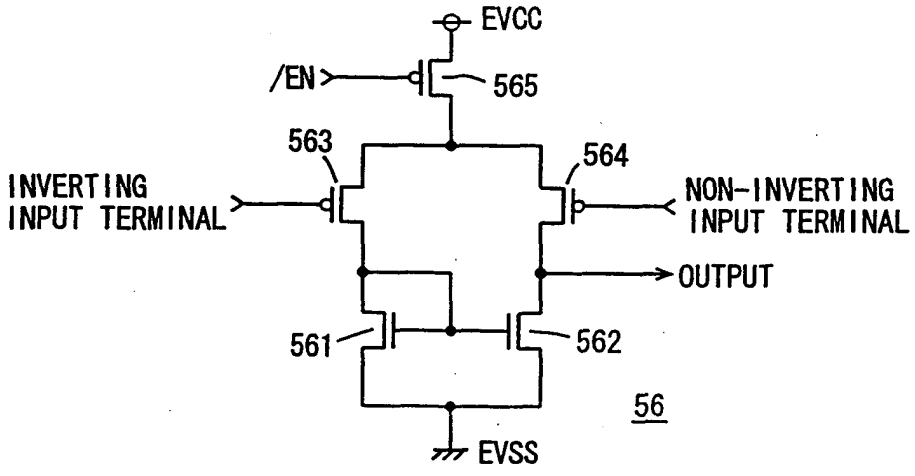


FIG. 5

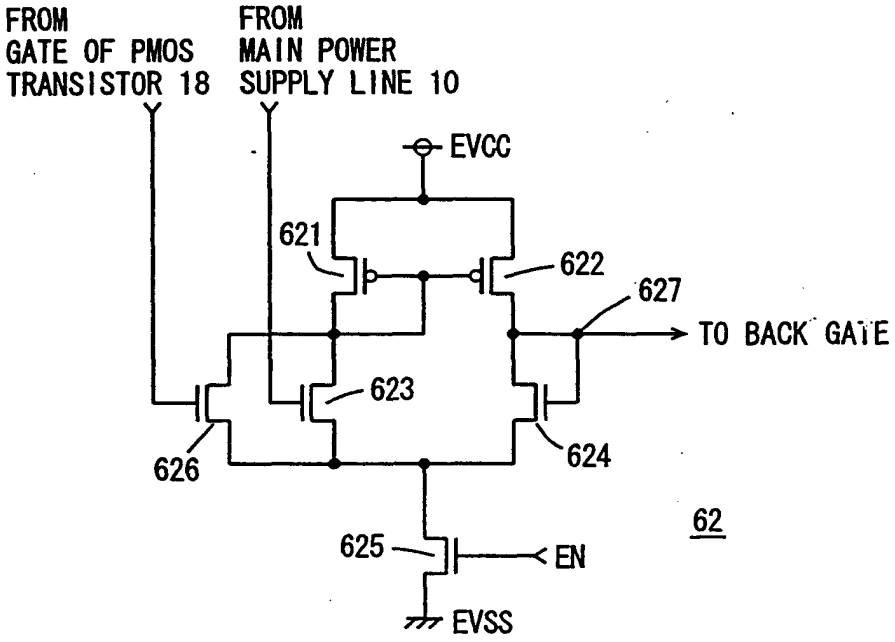

FROM
GATE OF PMOS
TRANSISTOR 18
FROM
MAIN POWER
SUPPLY LINE 10
EVCC
621
622
627
TO BACK GATE
623
626
624
625
EN
EVSS
62

FIG. 6

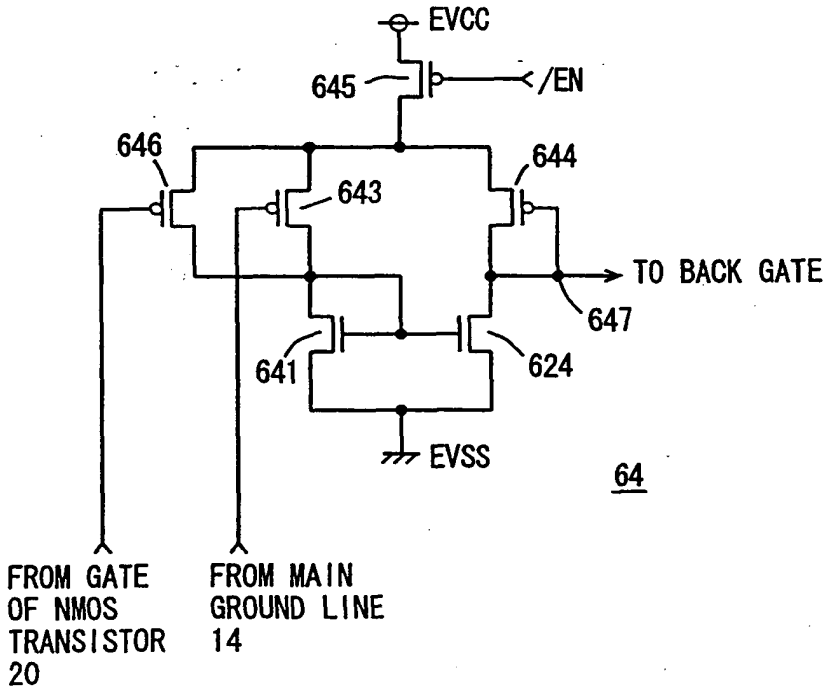

EVCC
645
/EN
646
644
643
TO BACK GATE
647
641
624
EVSS
64
FROM GATE
OF NMOS
TRANSISTOR
20
FROM MAIN
GROUND LINE
14

FIG. 7

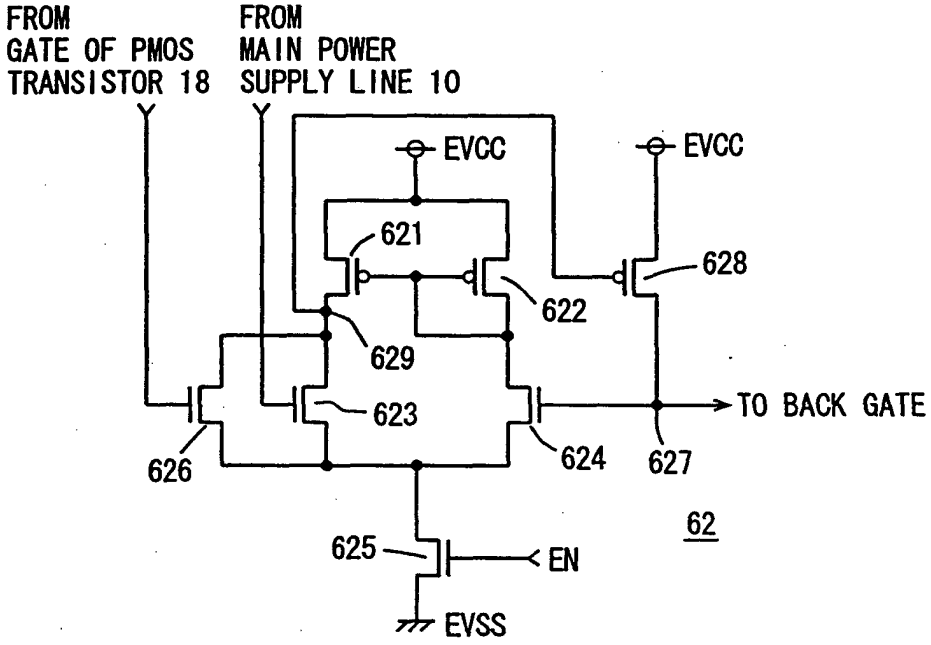

FROM
GATE OF PMOS
TRANSISTOR 18
FROM
MAIN POWER
SUPPLY LINE 10
EVCC
EVCC
621
628
622
629
623
TO BACK GATE
626
624
627
62
625
EN
EVSS

FIG. 8

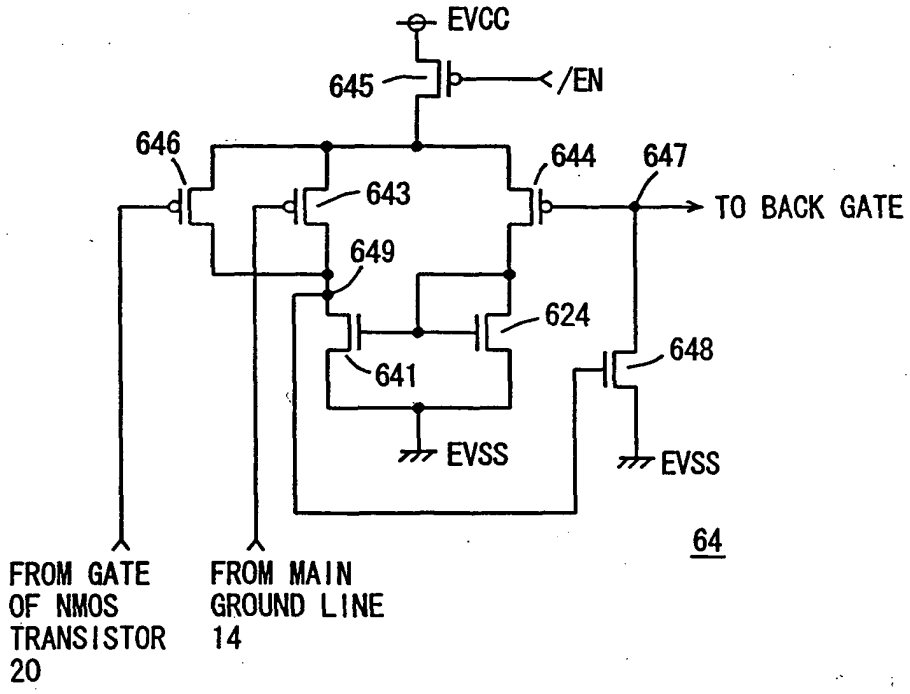

EVCC
645
/EN
646
644
647
643
TO BACK GATE
649
624
648
641
EVSS
EVSS
64
FROM GATE
OF NMOS
TRANSISTOR
20
FROM MAIN
GROUND LINE
14

FIG. 9

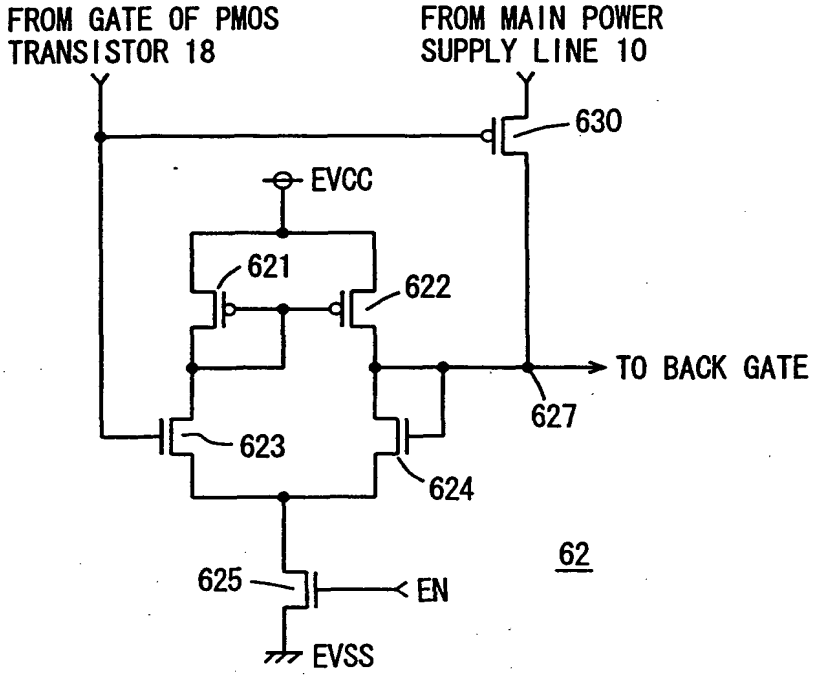

FROM GATE OF PMOS TRANSISTOR 18
FROM MAIN POWER SUPPLY LINE 10
630
EVCC
621
622
TO BACK GATE
627
623
624
62
625
EN
EVSS

FIG. 10

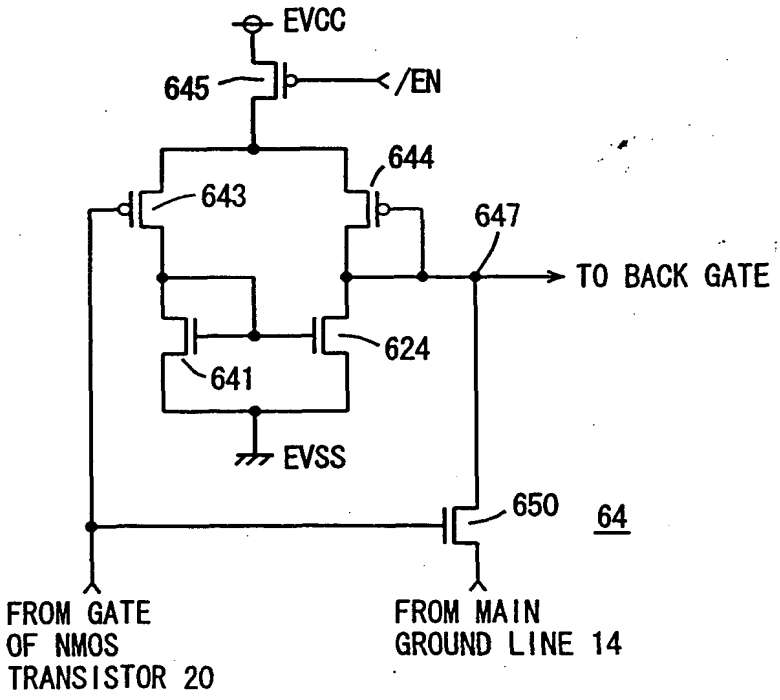

EVCC
645
/EN
644
643
647
TO BACK GATE
624
641
EVSS
650
64
FROM GATE OF NMOS TRANSISTOR 20
FROM MAIN GROUND LINE 14

FIG. 11

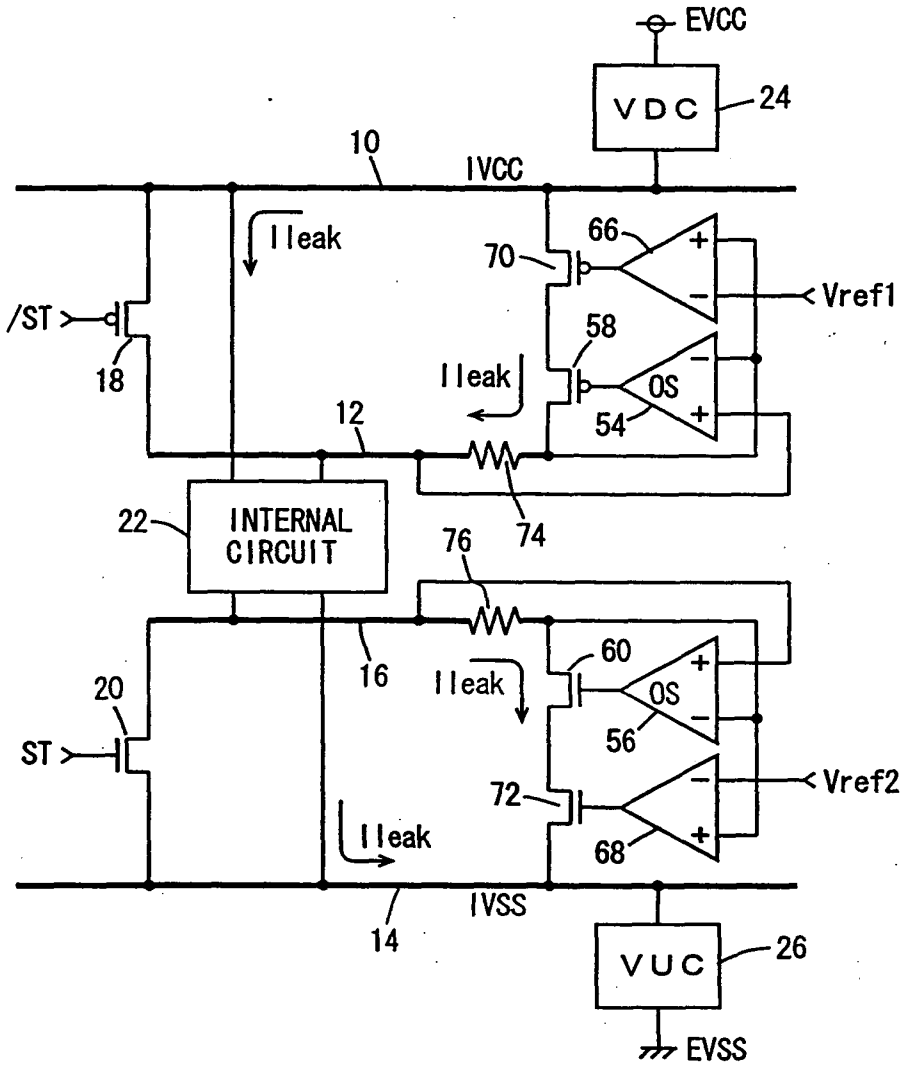

EVCC
VDC
24
10
IVCC
Ileak
66
70
Vref1
/ST
18
58
Ileak
OS
54
12
74
22
INTERNAL CIRCUIT
76
16
60
Ileak
OS
56
20
ST
72
Vref2
Ileak
68
IVSS
14
VUC
26
EVSS

FIG. 12

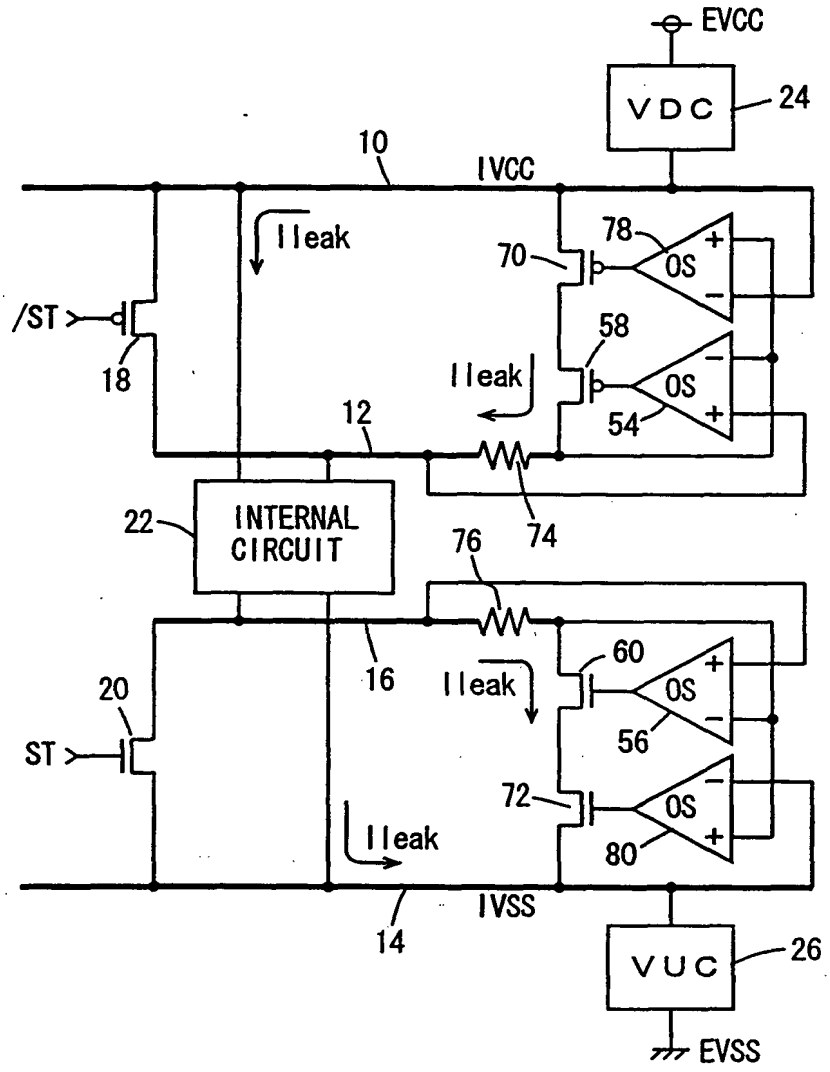
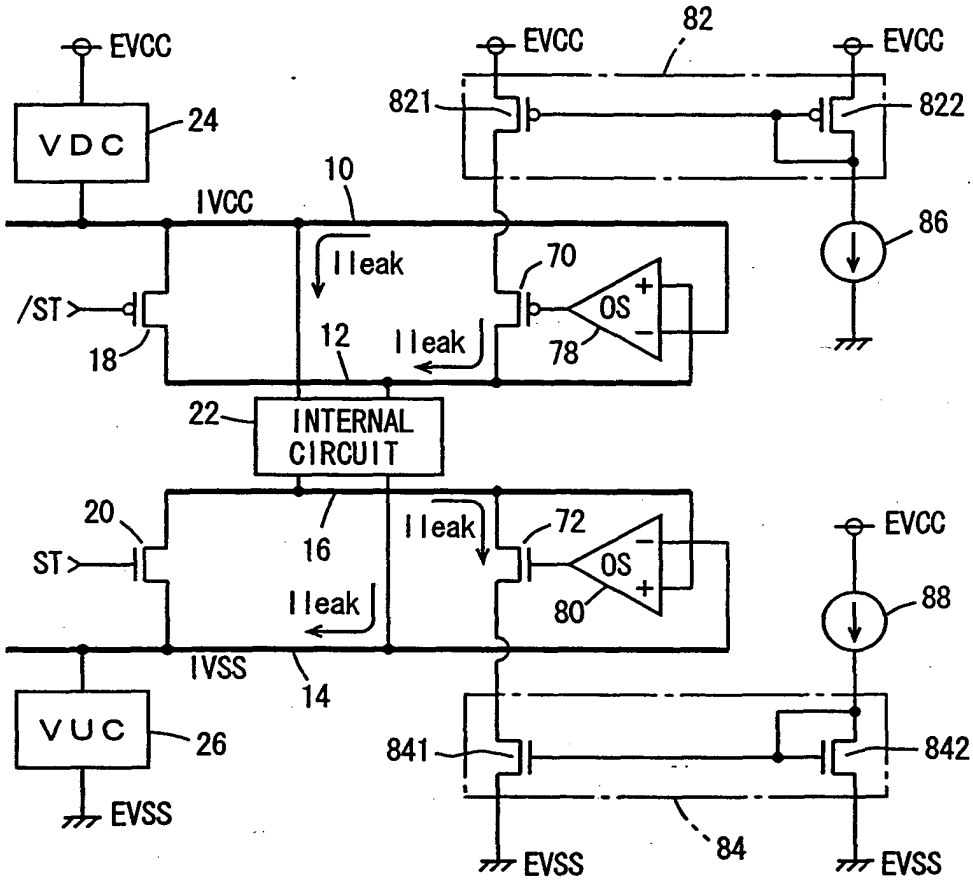

EVCC
VDC
24
10
IVCC
Ileak
78
70
OS
/ST
18
58
Ileak
OS
54
12
74
22
INTERNAL CIRCUIT
76
60
16
Ileak
OS
20
ST
56
72
OS
Ileak
80
IVSS
14
VUC
26
EVSS

FIG. 13


EVCC
VDC
24
IVCC
10
/ST
18
Ileak
12
Ileak
70
OS
78
EVCC
82
821
822
EVCC
86
22
INTERNAL CIRCUIT
20
ST
16
Ileak
72
OS
80
Ileak
EVCC
88
IVSS
14
VUC
26
EVSS
841
842
84
EVSS
EVSS

F I G. 1 4

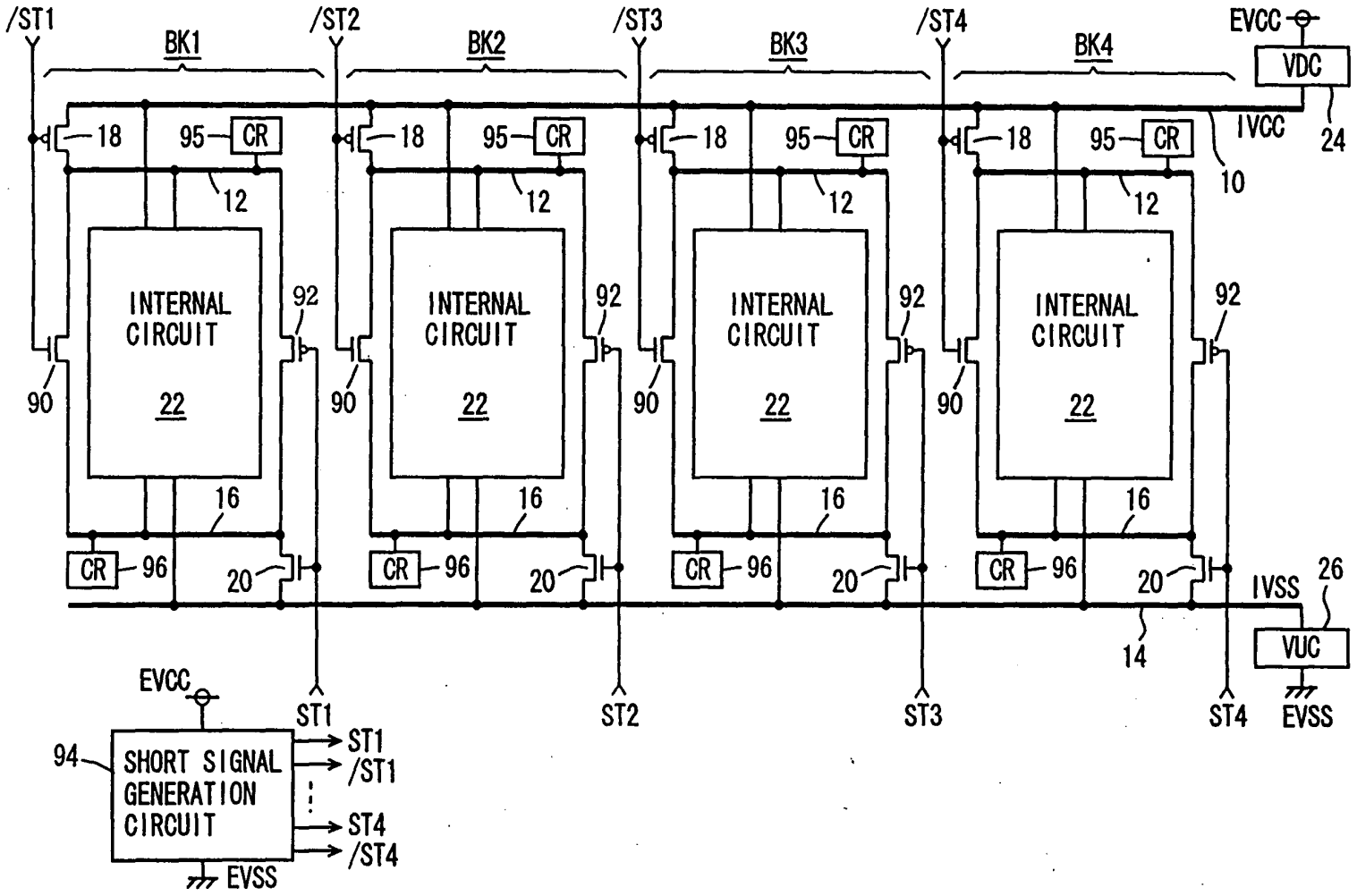

/ST1
/ST2
/ST3
/ST4
BK1
BK2
BK3
BK4
EVCC
VDC
IVCC
24
10
18
95
CR
12
INTERNAL CIRCUIT
22
92
90
16
96
20
IVSS
26
VUC
EVSS
14
ST1
ST2
ST3
ST4
94
SHORT SIGNAL GENERATION CIRCUIT
/ST1
/ST4

FIG. 15

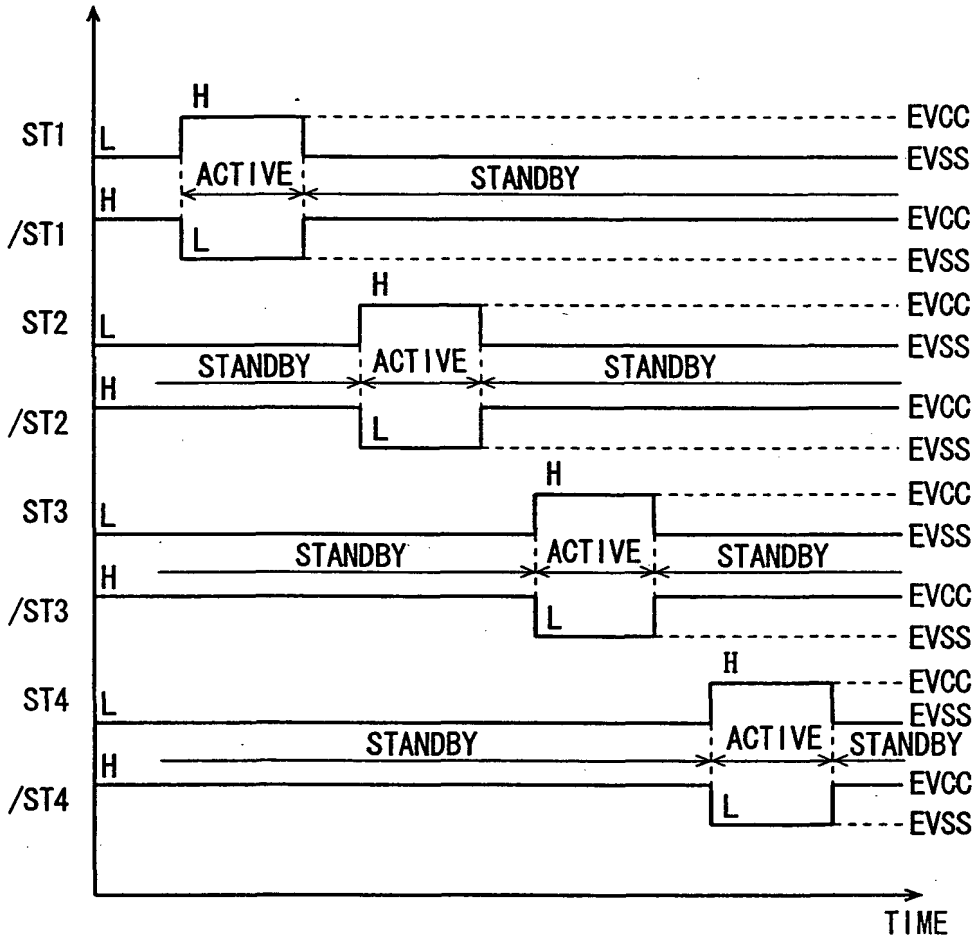

ST1
/ST1
ST2
/ST2
ST3
/ST3
ST4
/ST4
H
L
ACTIVE
STANDBY
EVCC
EVSS
TIME

FIG. 16

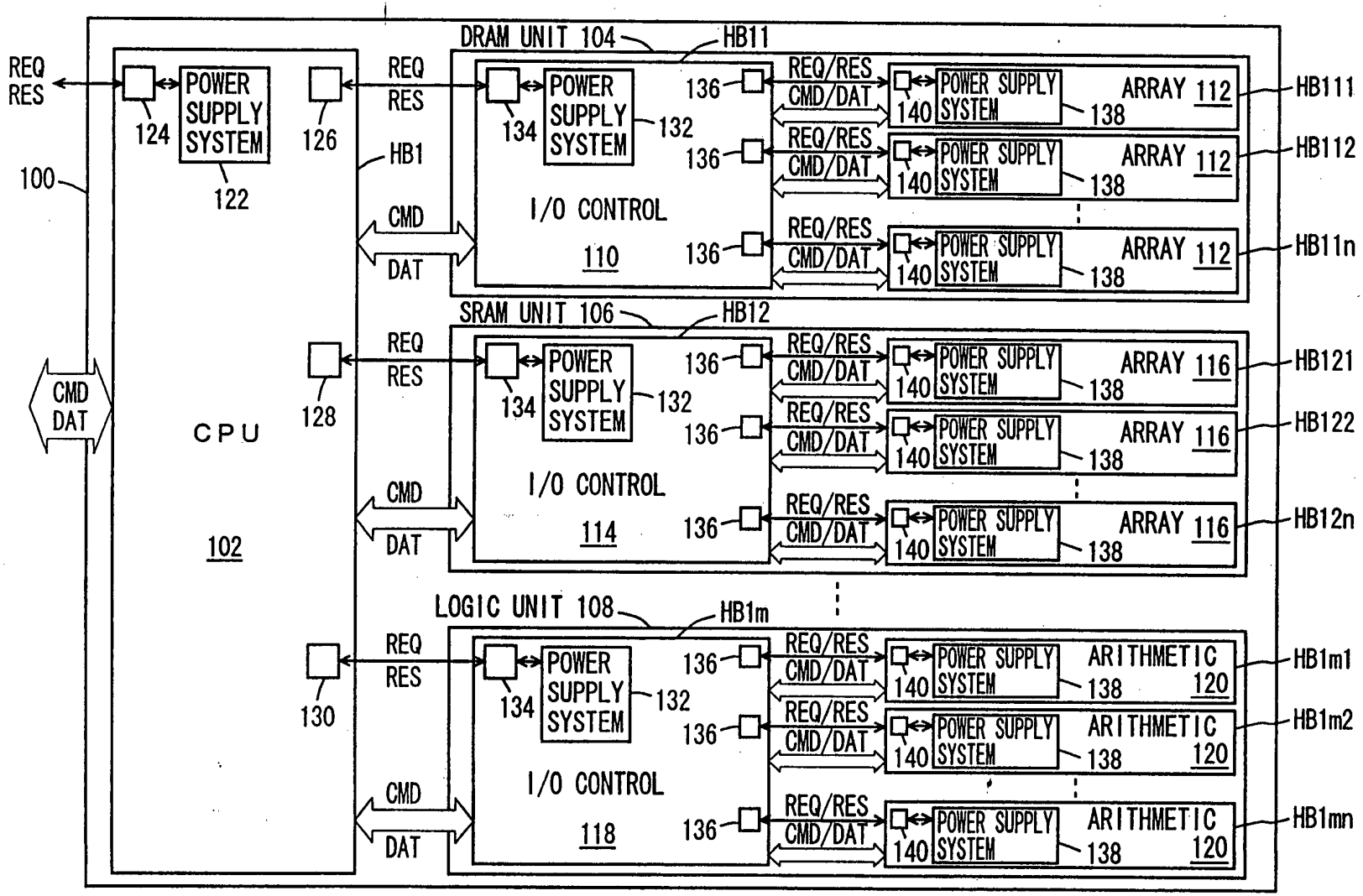

DRAM UNIT 104
HB11
SRAM UNIT 106
HB12
LOGIC UNIT 108
HB1m
REQ
RES
CMD
DAT
HB1
100
CPU
102
POWER SUPPLY SYSTEM
124
122
126
128
130
134
132
136
140
138
I/O CONTROL
110
114
118
REQ/RES
CMD/DAT
ARRAY 112
ARRAY 116
ARITHMETIC 120
HB111
HB112
HB11n
HB121
HB122
HB12n
HB1m1
HB1m2
HB1mn

FIG. 17

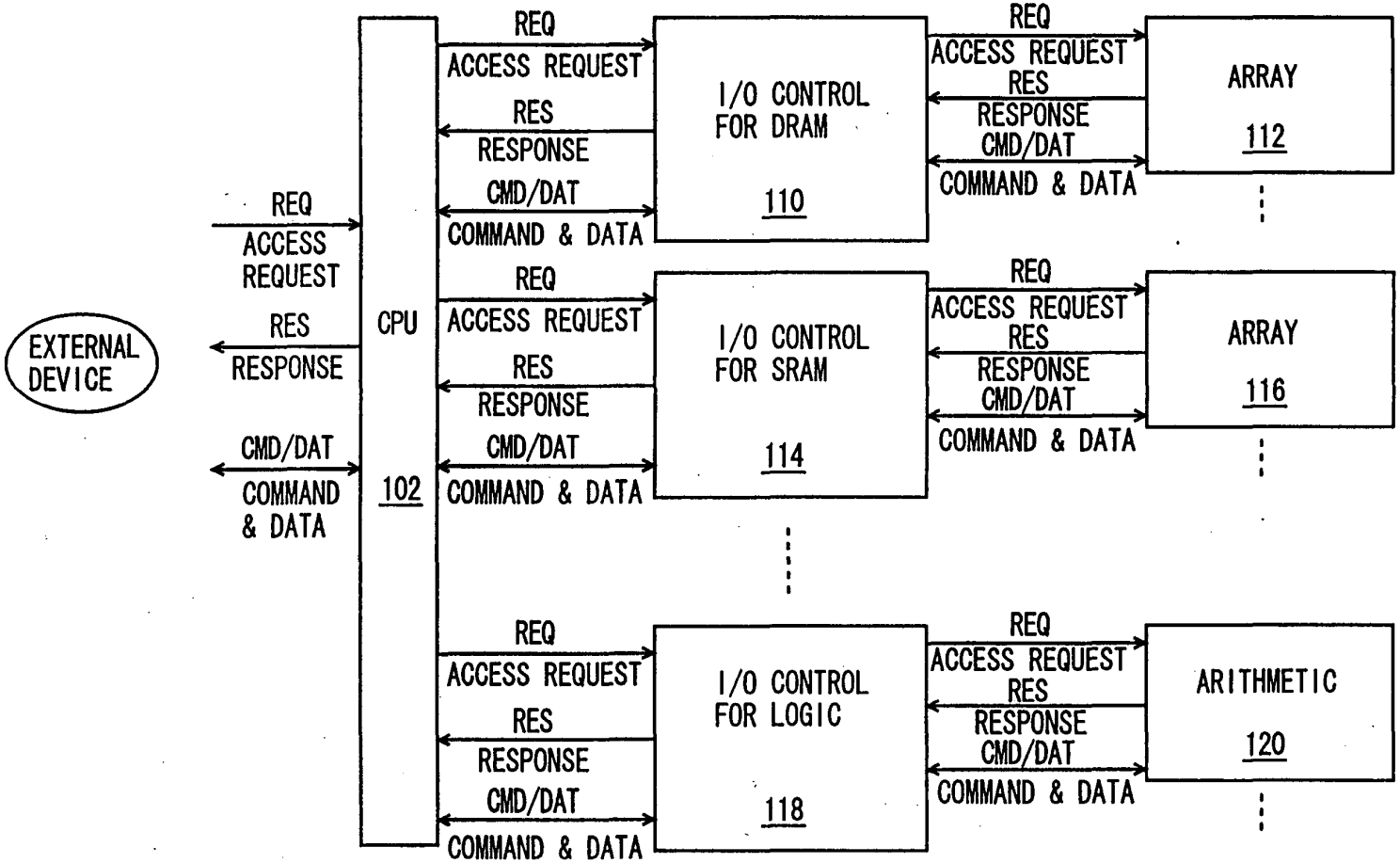

EXTERNAL DEVICE
REQ
ACCESS REQUEST
RES
RESPONSE
CMD/DAT
COMMAND & DATA
CPU
102
REQ
ACCESS REQUEST
RES
RESPONSE
CMD/DAT
COMMAND & DATA
I/O CONTROL FOR DRAM
110
I/O CONTROL FOR SRAM
114
I/O CONTROL FOR LOGIC
118
ARRAY
112
ARRAY
116
ARITHMETIC
120

FIG. 18

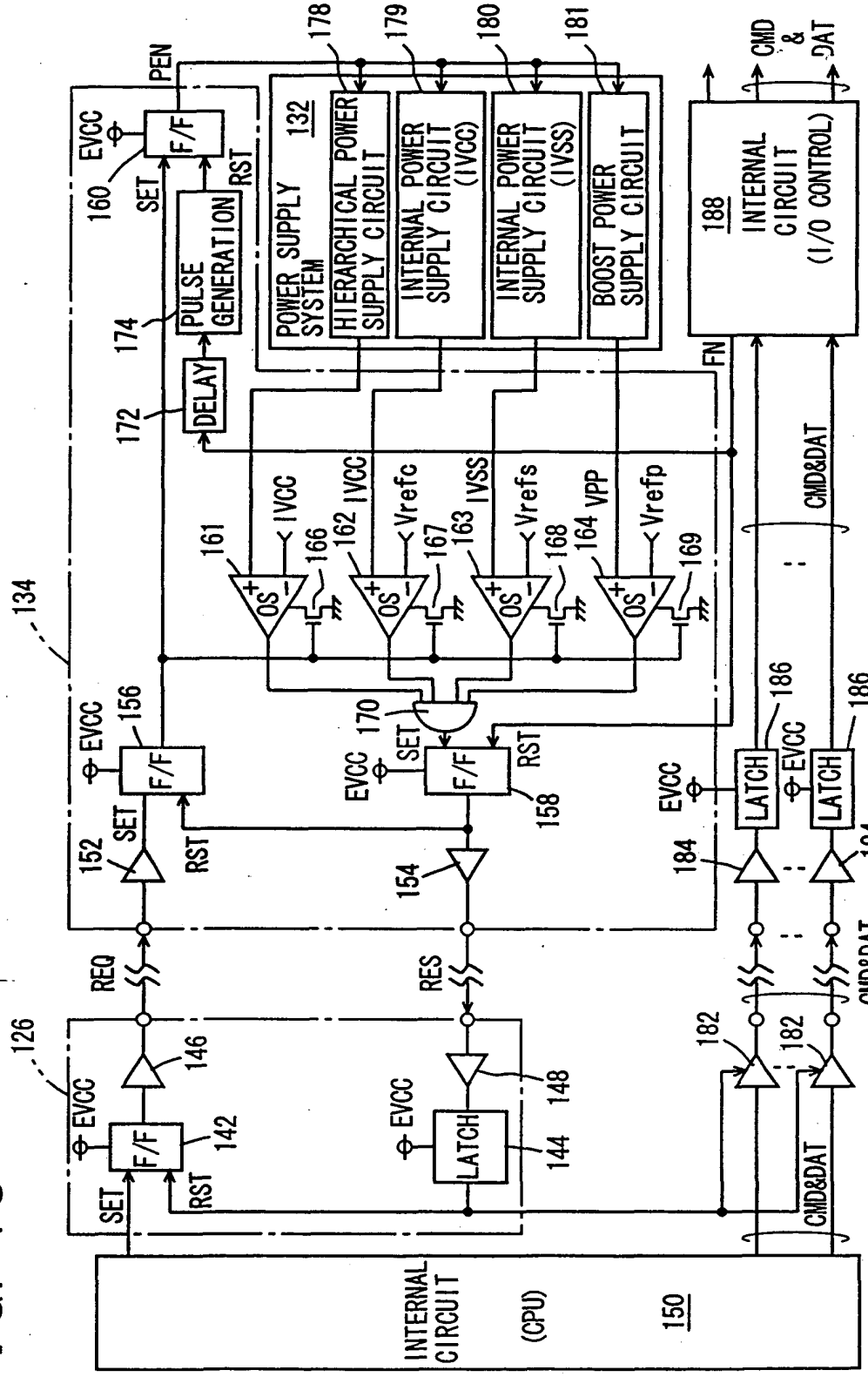

INTERNAL CIRCUIT (CPU) 150
126
134
REQ
RES
CMD&DAT
SET
RST
EVCC
F/F
LATCH
PEN
DELAY
PULSE GENERATION
POWER SUPPLY SYSTEM 132
HIERARCHICAL POWER SUPPLY CIRCUIT
INTERNAL POWER SUPPLY CIRCUIT (IVCC)
INTERNAL POWER SUPPLY CIRCUIT (IVSS)
BOOST POWER SUPPLY CIRCUIT
188 INTERNAL CIRCUIT (I/O CONTROL)
CMD & DAT
FN
IVCC
Vrefc
IVSS
Vrefs
VPP
Vrefp
OS
146
148
142
144
152
154
156
158
160
161
162
163
164
166
167
168
169
170
172
174
178
179
180
181
182
184
186

FIG. 19

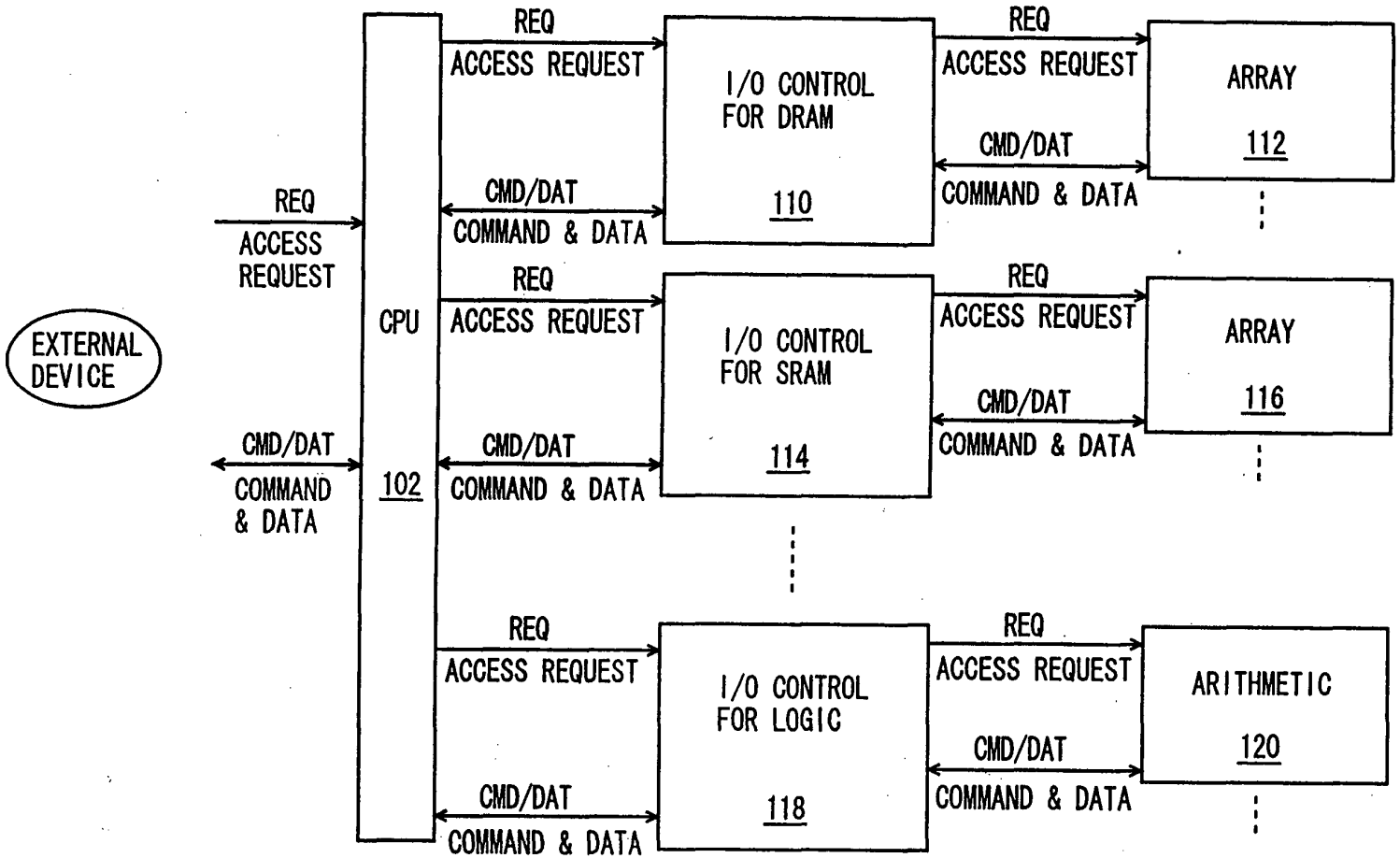

EXTERNAL DEVICE
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
CPU
102
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
I/O CONTROL FOR DRAM
110
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
ARRAY
112
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
I/O CONTROL FOR SRAM
114
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
ARRAY
116
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
I/O CONTROL FOR LOGIC
118
REQ
ACCESS REQUEST
CMD/DAT
COMMAND & DATA
ARITHMETIC
120

FIG. 20

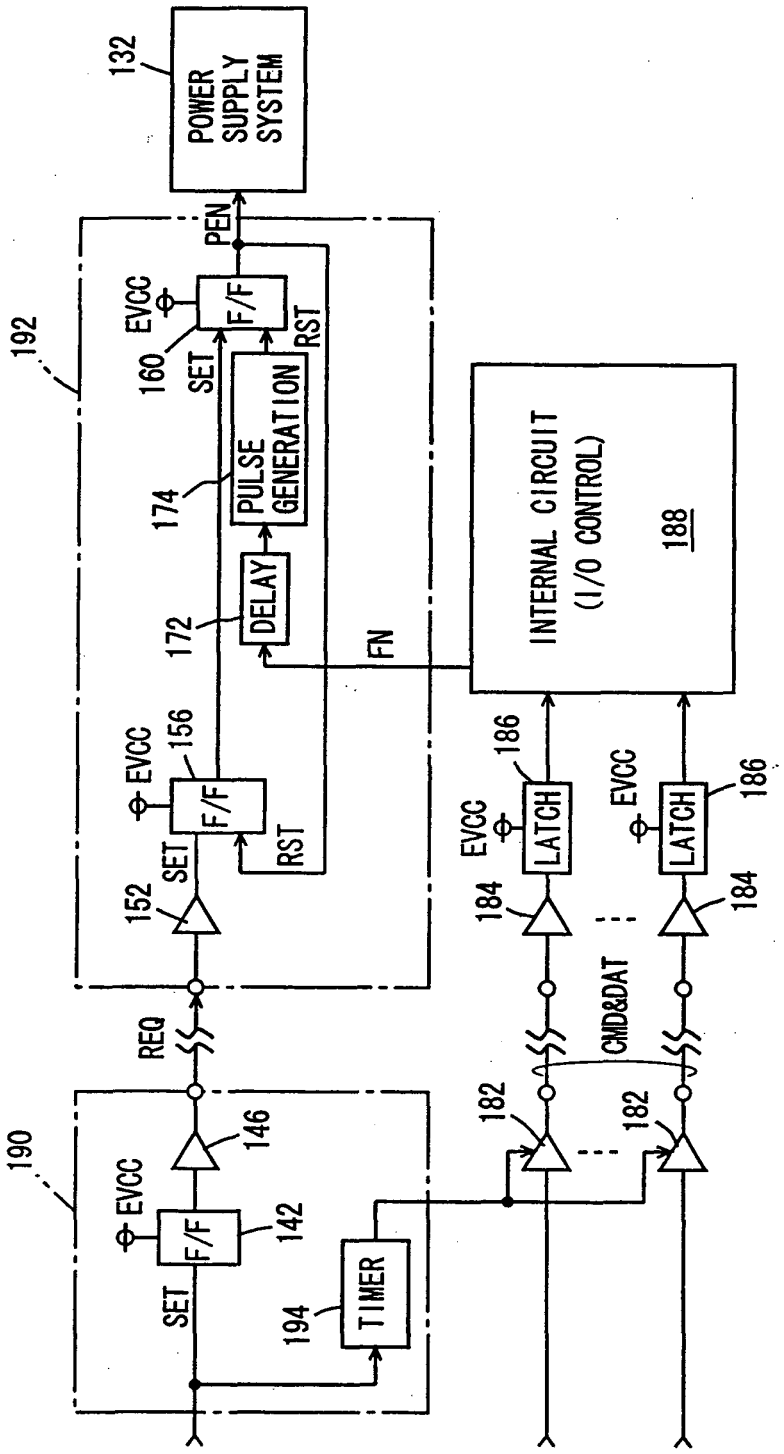

132
POWER SUPPLY SYSTEM
PEN
192
EVCC
160
SET
F/F
RST
174
PULSE GENERATION
172
DELAY
FN
EVCC
156
SET
F/F
RST
152
REQ
190
EVCC
SET
F/F
142
146
194
TIMER
INTERNAL CIRCUIT (I/O CONTROL)
188
EVCC
186
LATCH
184
EVCC
186
LATCH
184
CMD&DAT
182
182

FIG. 21

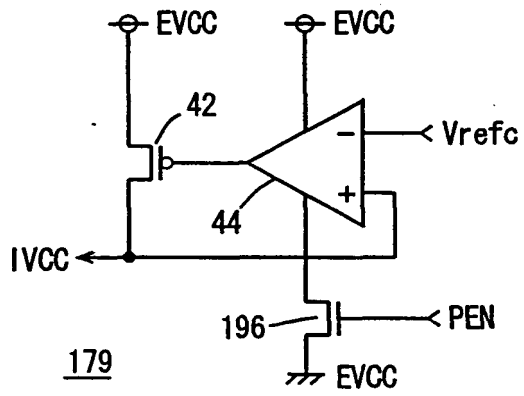

EVCC
EVCC
42
Vrefc
44
IVCC
196
PEN
179
EVCC

FIG. 22

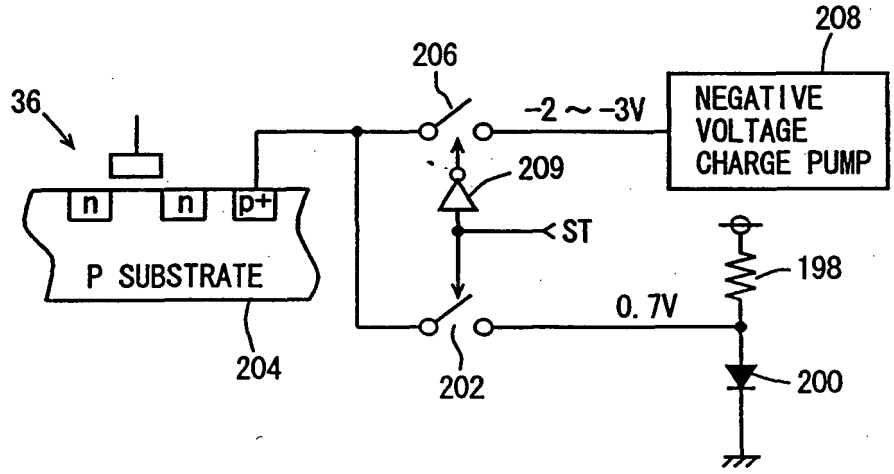

208
206
36
-2 ~ -3V
NEGATIVE VOLTAGE CHARGE PUMP
209
ST
198
n
n
p+
P SUBSTRATE
0.7V
204
202
200

FIG. 23

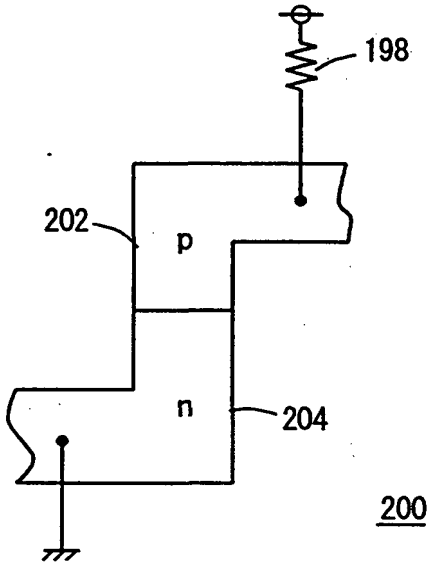
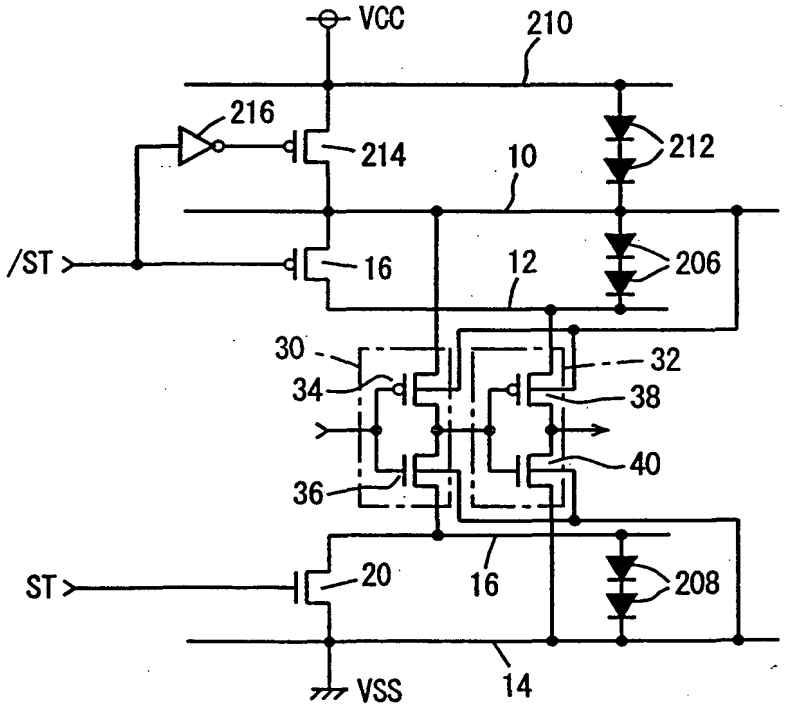

198
202
p
n
204
200

FIG. 24


VCC
210
216
214
212
10
/ST
16
12
206
30
32
34
38
40
36
ST
20
16
208
VSS
14